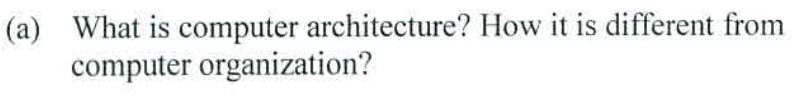
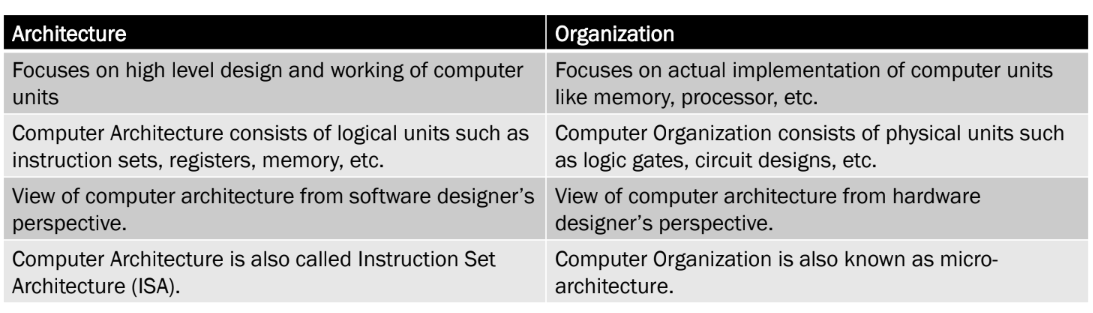
**AUTUMN END SEMESTER EXAMINATIONS-2023**

**SCHEME OF EVALUATION**

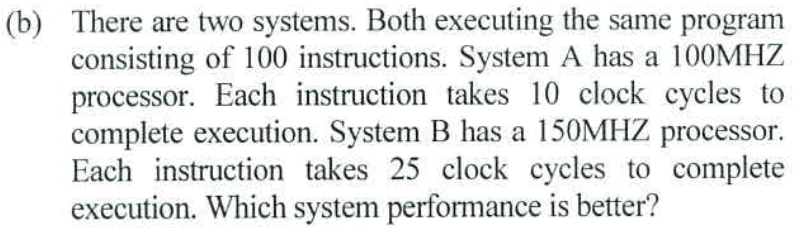
**SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE(IT-21002)**

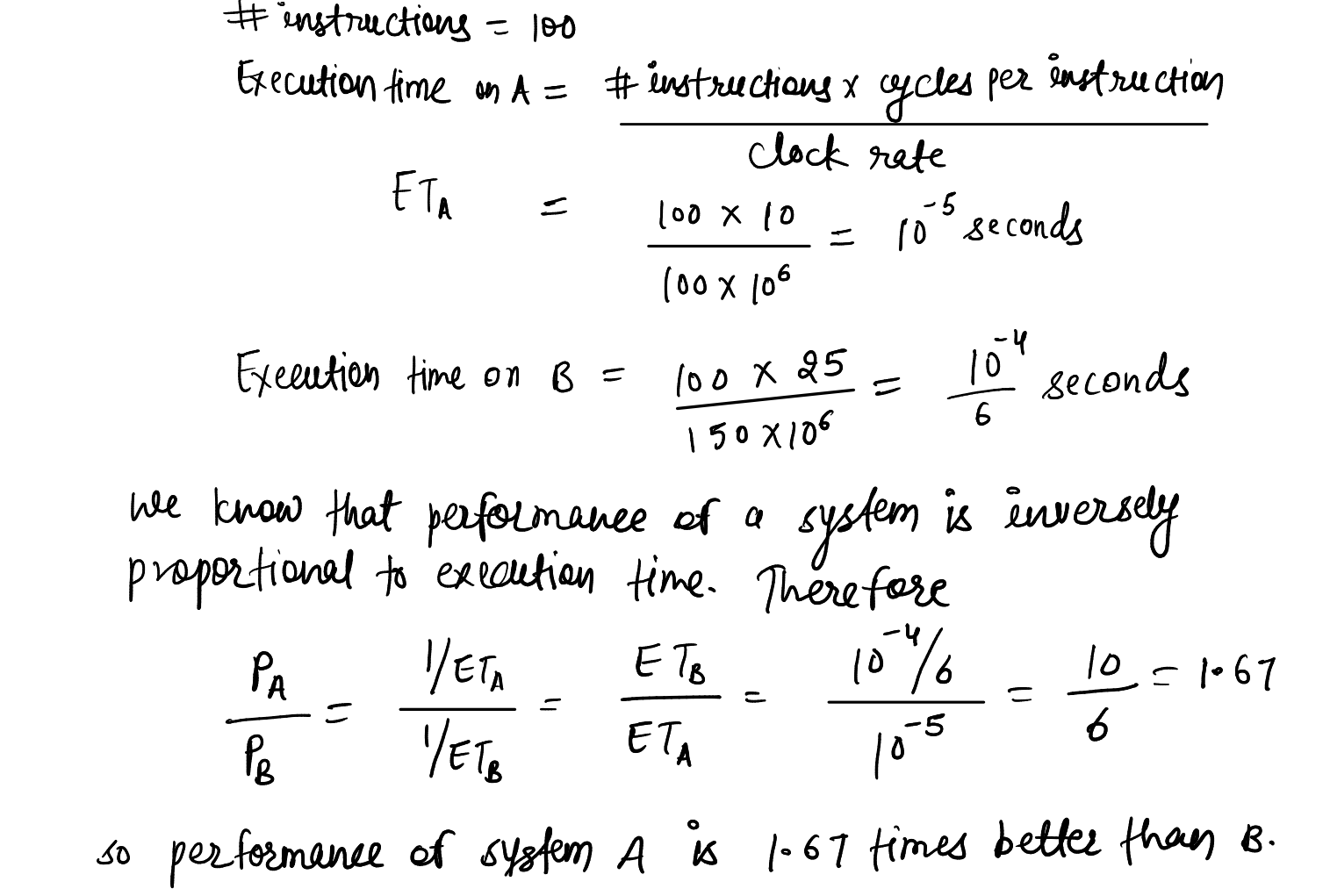
**Branch: IT, CSSE Total Marks: 50**

Q1

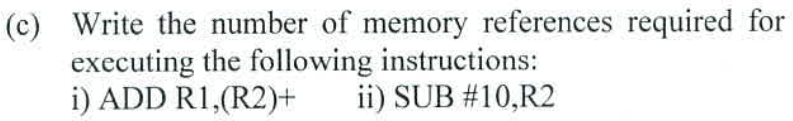


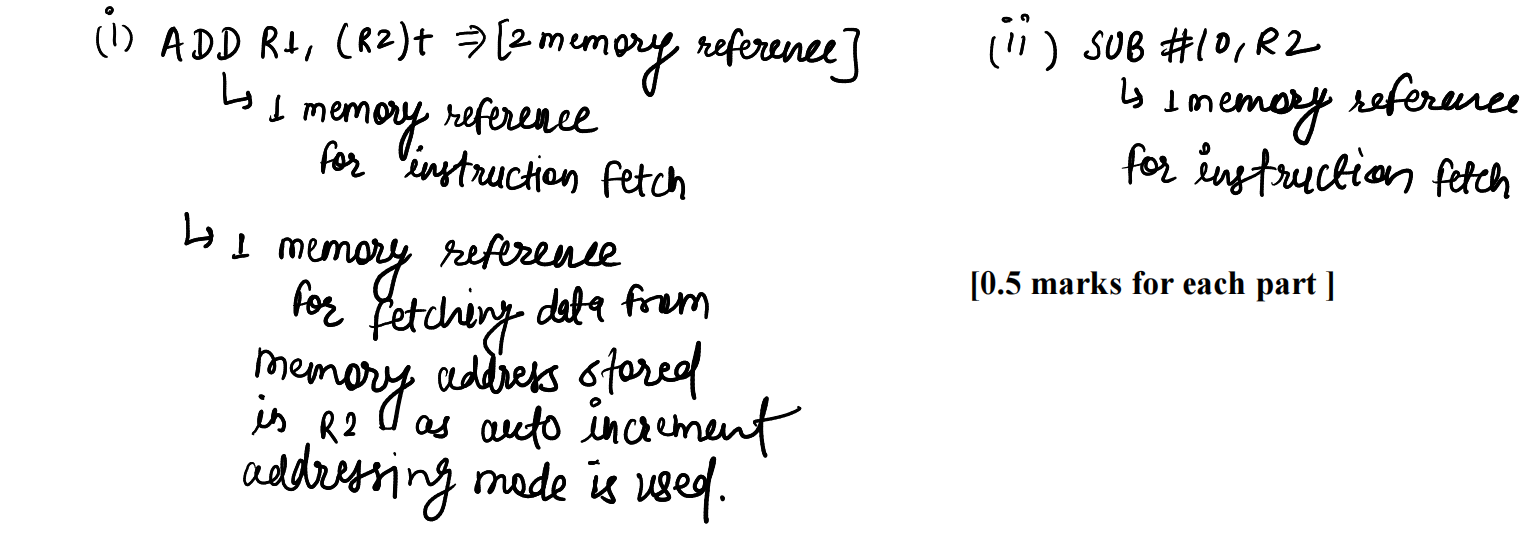
**[1 mark for correct answer. Partial marks can be awarded.]**





**[1 mark for correct answer with proper explaination]**





**(i)ADD R1,(R2)+** [3 memory references if 2nd operand is the destination]

(d)What is the use of WMFC signal in memory fetch operation?

**The WMFC (Wait for Memory-Function-Completed) signal causes the processor waits for the arrival of the MFC signal.When memory READ operation is completed then WMFC signal is generated.**

**[1 mark for correct answer. Partial marks can be awarded.]**

(e )A processor has 180 distinct instructions and 40 general-purpose registers. A 32 bit instruction word has an opcode, two register operands and an immediate operand. How many bits are available for the immediate operand field?

|  |  |  |  |
| --- | --- | --- | --- |
| **Opccode=8** | **Register=6** | **Register=6** | **Immediate operand=12** |

**[1 mark for correct answer with proper explaination]**

(f)A processor advertised as having a 900 MHz clock is always provides better performance than a 700-MHz processor (True/False). Justify your answer.

**False,because both processor may have a different value of S.**

**T=(N\*S)/R**

(g)How many 64 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

**No of chip=(2048\*8) /(64\*8)=32**

**[1 mark for correct answer. Partial marks can be awarded.]**

(h)A cache has 95% hit ratio, an access time of 100ns on cache hit and access time of 800ns on cache miss. Compute the effective access time of cache memory.

**Tavg=hc+(1-h)M**

**=o.95\*100+0.05\*800**

**=135ns**

**[1 mark for correct answer with proper explaination]**

1. Find the number of gate delays for obtaining C20(Carry-20) in the following 20-bit carry-look ahead adder built from five 4-bit adders.

C20=3+2+2+2+2=11gate delay

**[1 mark for correct answer. Partial marks can be awarded.]**

(j)Distinguish between cycle stealing and burst mode data transfer in DMA .

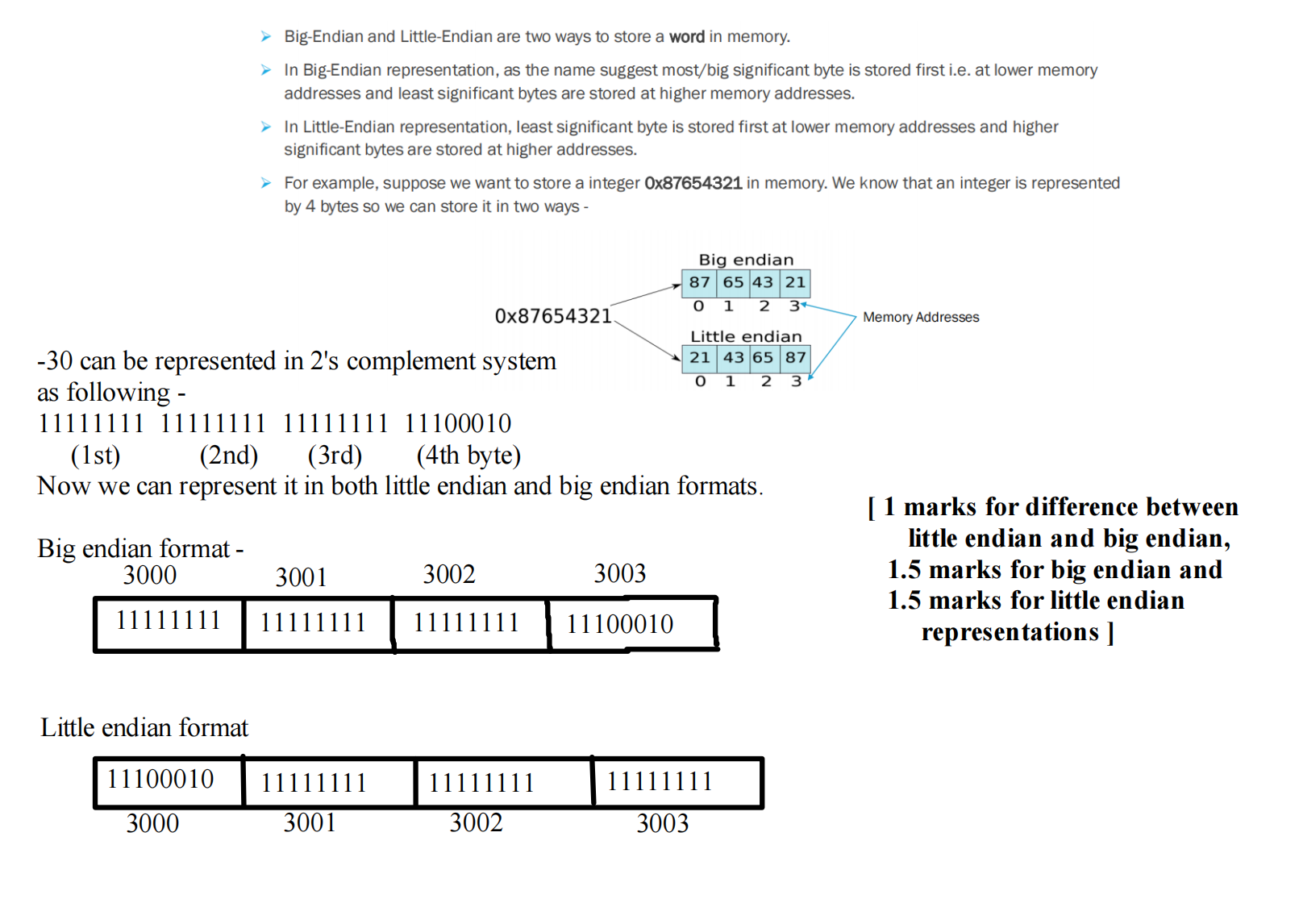
(1)Burst mode DMA transfers data in a continuous sequence, while cycle stealing DMA temporarily takes control of the system bus to transfer smaller amounts of data before returning control to the CPU.

(2) Burst mode is used for faster device,while cycle stealing is used for slower device.

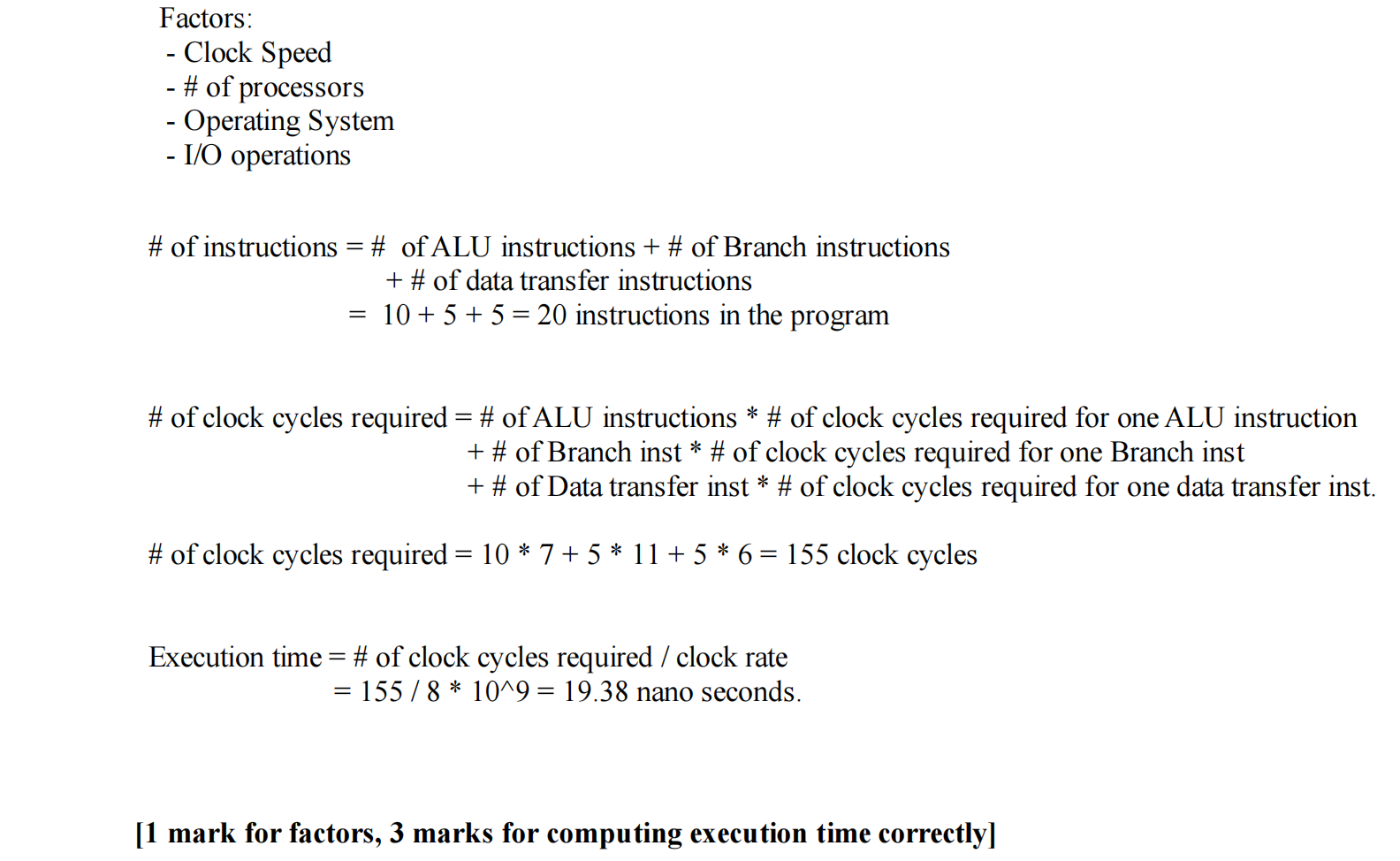
**[1 mark for correct answer. Partial marks can be awarded.]**

**SECTION-B**

Q2(a**).**Differentiate big endian and little endian address assignment schemes. Represent the number “-30” in little and big endian style. Assuming the memory locations starts at the address 3000 and the memory is byte-addressable memory organized in 32-bit words.



(b)Discuss the factors that affect the performance of the computer. If a 8GHz computer takes 7 clock cycles for ALU instructions, 11 clock cycles for branch instructions and 6 clock cycles for data transfer instructions. Then Find the total time taken by the computer to execute the program that consists of 10 ALU instructions, 5 branch instructions and 5 data transfer instructions



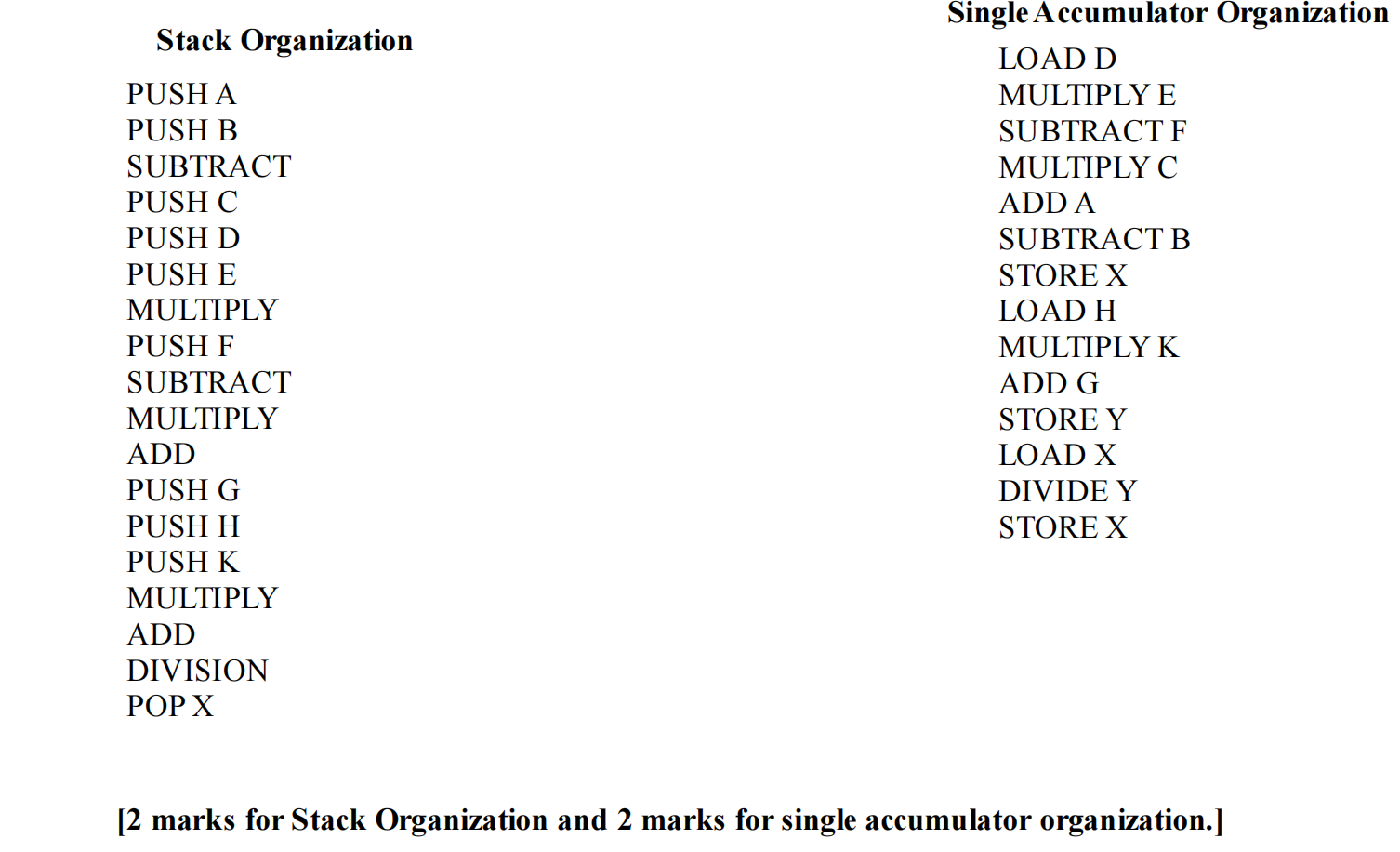
Q3(a)Write a program to evaluate the arithmetic statement:

X = (A-B+C\*(D\*E-F)) / (G+H\*K)

i) Using a stack organized computer with zero-address operation instructions.

ii) Using an accumulator type computer with one address instructions.

iii) Using a general register computer with two address instructions



(b)What is the use of addressing mode? Difference between indirect and register indirect addressing mode. Write the assembly language code to execute the C-language statement A = \*B, using indirect and register indirect addressing mode where B is a pointer variable.

**Addressing modes** are different ways to specify memory location from where data needs to be fetched for that instruction.

**Indirect** - In indirect addressing mode, memory location (address) specified in the instruction stores the address of memory location from where data needs to be fetched.

**Register Indirect** - In register indirect addressing mode, register specified in the instruction stores the address of memory location from where data needs to be fetched.

**A = \*B**

**Indirect addressing mode**

MOVE (B),A [2nd operand is the destination]

**Register Indirect addressing mode**

MOVE B,R1 [2nd operand is the destination]

MOVE (R1),A [2nd operand is the destination]

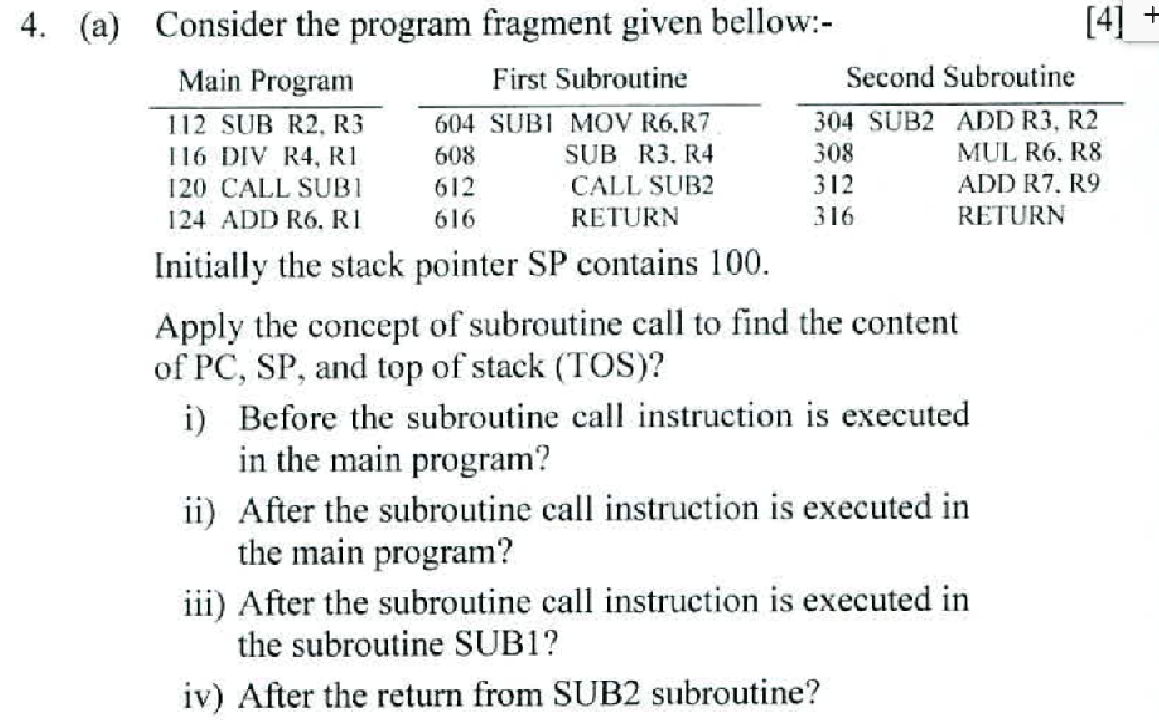
**[1 mark for addressing mode definition / use**

**1 mark for difference memory indirect / indirect and register indirect addressing modes**

**1 mark for assembly code of indirect mode**

**1 mark for assembly code of register indirect mode]**

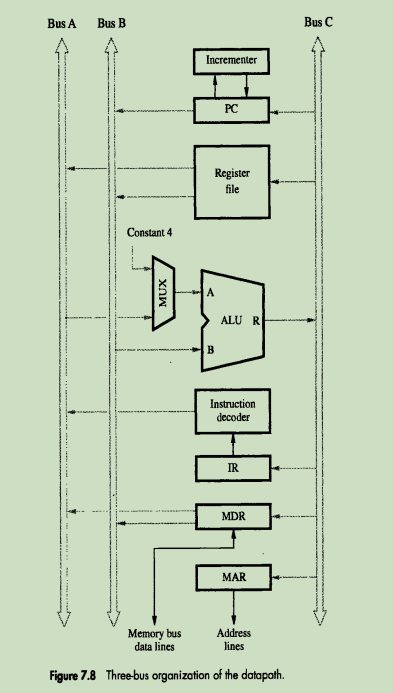
**SECTION-C**

**Q4(a)**

1. **PC=124 SP=100 TOS=[100] [1]**
2. **PC=604 SP=96 TOS=124 [1]**
3. **PC=304 SP=92 TOS=616 [1]**
4. **PC=616 SP=96 TOS=124 [1]**

(b)Explain the 3-bus architecture inside CPU with neat diagram. Write the control signals for the following instruction. [10 Marks]

MUL (R1) , R5



**MUL 5(R1),R5**

1. **PCout,R=B,MARin,Read,Inc.PC**
2. **WMFC**
3. **MDAoutB,R=B,IRin**
4. **Offset field of IRout,R1outB,Select A,ADD,MARin,Read**
5. **WMFC**
6. **R1outA,MDRoutB,Select A,MUL,R5in,end**

[Diagram and explanation 2mark and control step 2mark]

Q5(a)Write the sequence of control steps for the following instructions for single bus CPU organization

I. I1: ADD 10(R3), R4

II. I2: Branch<0 L1

III. I3: MUL -(R5), R5

Design the logic function for WMFC control signal with reference to the above instructions i.e. I1 to I3.

**I1 :ADD 10(R3), R4**

1. PCout,MARin,READ,select4,ADD,Zin
2. Zout,Pcin,Yin,WMFC
3. Zout,IRin
4. Offset field of IRout,Yin
5. R3out,Seiect Y,ADD,Zin
6. Zout,MARin,Read,
7. R4out,Yin,WMFC
8. MDRout,Select Y,ADD,Zin
9. Zout,R4in.end

**I2:Branch<0 L1**

1.PCout,MARin,READ,select4,ADD,Zin

2.Zout,Pcin,Yin,WMFC

3.Zout,IRin

Execution stage do not have memory operation

I3: MUL -(R5), R5

1.PCout,MARin,READ,select4,ADD,Zin

2.Zout,Pcin,Yin,WMFC

3.Zout,IRin

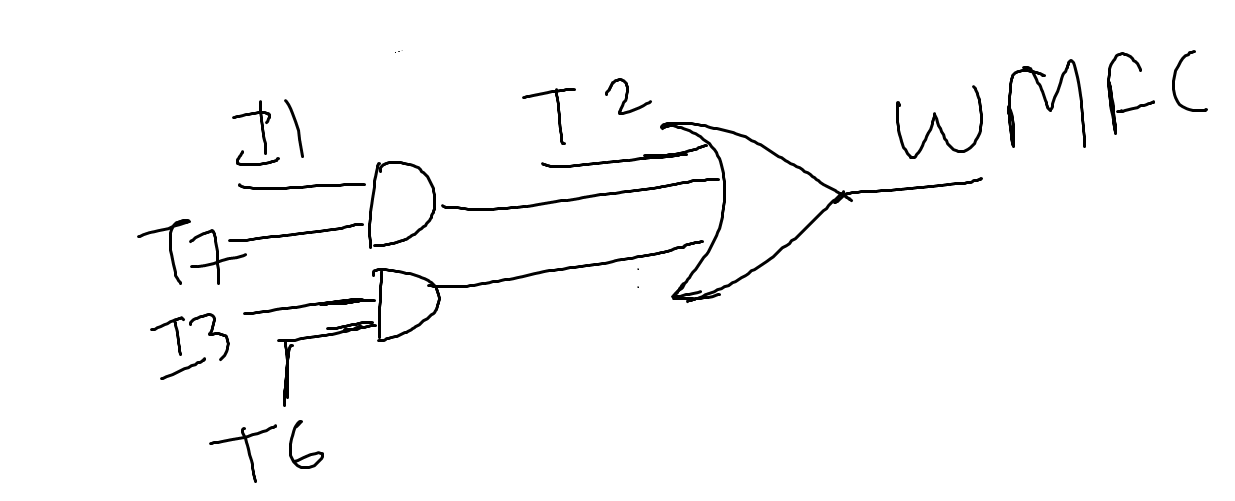
4.R5out,Select 4,SUB,Zin

5.Zout,R5in,MARin,Read

6.R5out,Yin,WMFC

7.MDRout,SelectY,MUL,Zin,R5in,end

WMFC=T2+I1.T7+I3.T6+………..



[Control step for each instruction 1mark and design of logic circuit 1mark]

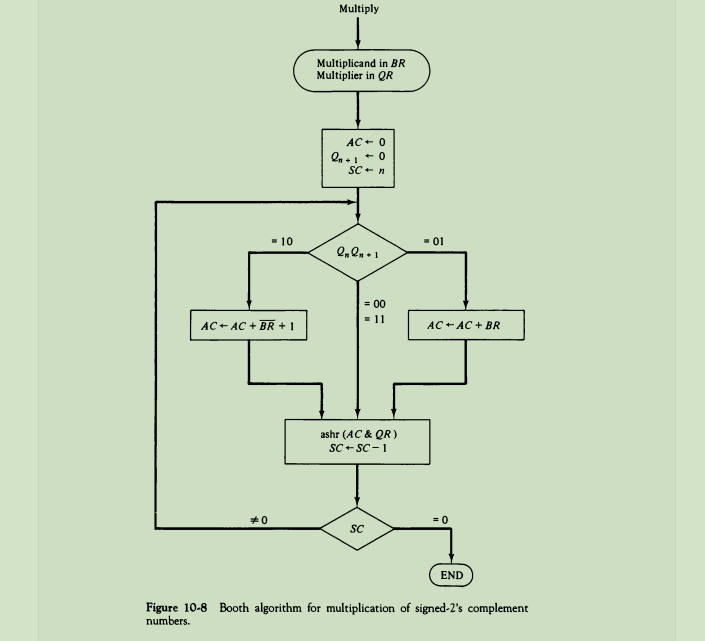
(b)Write the function of control unit. Explain the following terms related to micro-programmed control unit design:

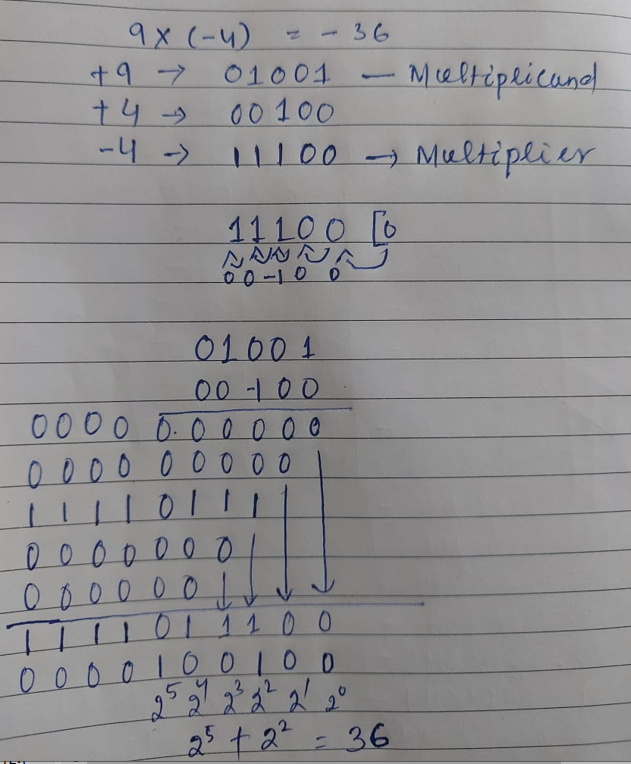
(i) Micro program counter (ii) Micro Routine

(iii) Micro Instruction (iv) Control Store

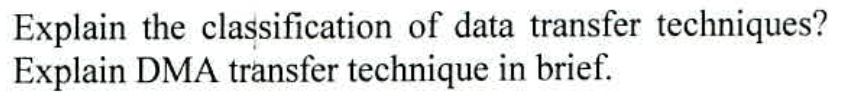
**[1 mark for each correct answer. Partial marks can be awarded.]**

Q6(a)Write the steps for multiplication according to Booth Multiplication.Explain with the example to multiply 9 with *-4.*





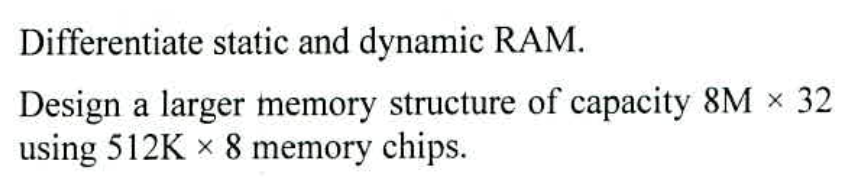
**[Both the method be considered**.**Partial marks can be awarded]**

(b)

Classification of data transfer. [1]

Explanation of DMA. [3]

[**Partial marks can be awarded]**

7(a)

Differentiation of SRAM and DRAM. [2]

Design [2]

**[Partial marks can be awarded]**

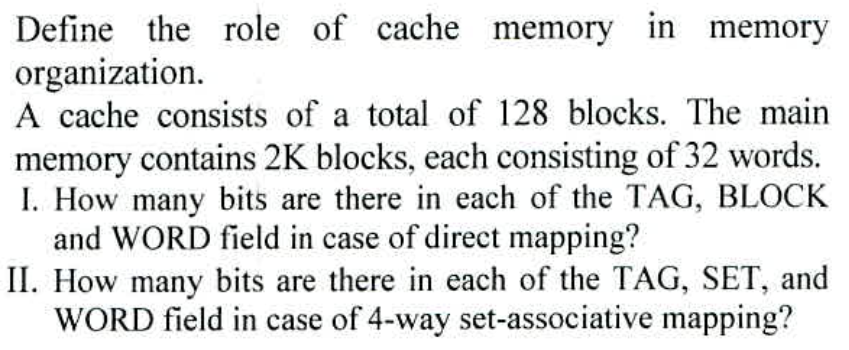
No of chip=64 Decoder size=4:16

Common address line=A0 to A18 Chip selection line=A19 to A22

Each word line have 4 no of chip

Data line partition:

D0-D7 D8-D15 D16-D23 D24-D31

(b)

Importance of cache memory in memory organization. [2]

(i)Direct mapping

|  |  |  |
| --- | --- | --- |
| TAG=4 | BLOCK=7 | WORD=5 |

(ii)4-way set-associative mapping

|  |  |  |
| --- | --- | --- |
| TAG=6 | SET=5 | WORD=5 |

Q8(a)Compare direct, set associative and fully associative mapping techniques.

Consider a 2-way set associative cache memory with 4 sets and a total 8 cache blocks (0-7) and a main memory with 128 blocks (0-127). What memory block will be present in the cache after the following sequence of memory references if LRU and FIFO policy is used for block replacement?

0 5 3 9 7 0 16 55

Comparision [2]

Solution of problem [2]

**[Partial marks can be awarded]**

* **Direct Mapped:** Each block has only one place that it can appear in the cache.

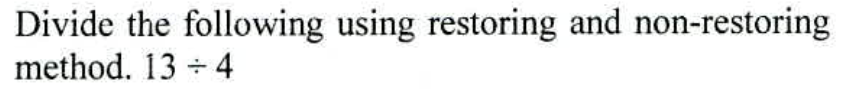
**Cache Block no = (Memory Block number) mod (No. of blocks in cache)**

* **Fully associative:** Each block can be placed anywhere in the cache.
* **Set associative:** Each block can be placed in a restricted set of places in the cache.
  + If there are n blocks in a set, the cache placement is called n-way set associative ( eg. 2 block in a set means 2 way set associative)

**Cache Set no. = (Memory Block address) mod (No. of sets in cache)**



(b)



Dividend=13 Divisor=4

(13)10=(1101)2 (4)10=(0100)2

Initial: A=0000 Q=1101(Dividend)

M=0100(Divisor) M’=1100

SC=4(total no of cycle)

RESULT: Quotient=0011 (3)

Remainder=0001 (1)

In Non-Restoring 2nd step is not required.

Restoring [2]

Non-Restoring [2]

**[Partial marks can be awarded]**